

FIG. 1

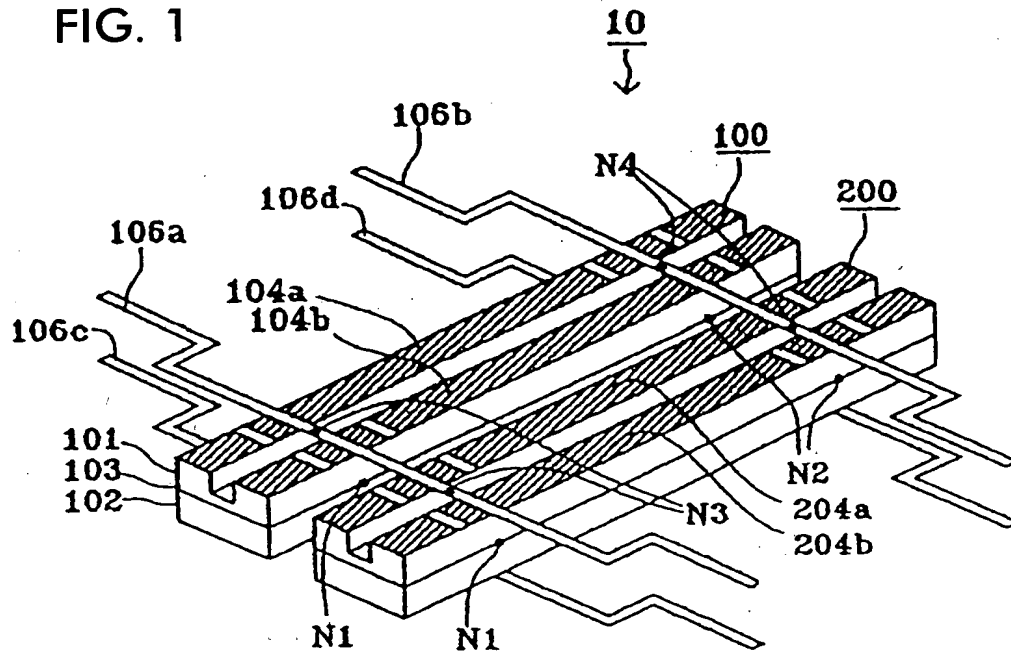


FIG. 4

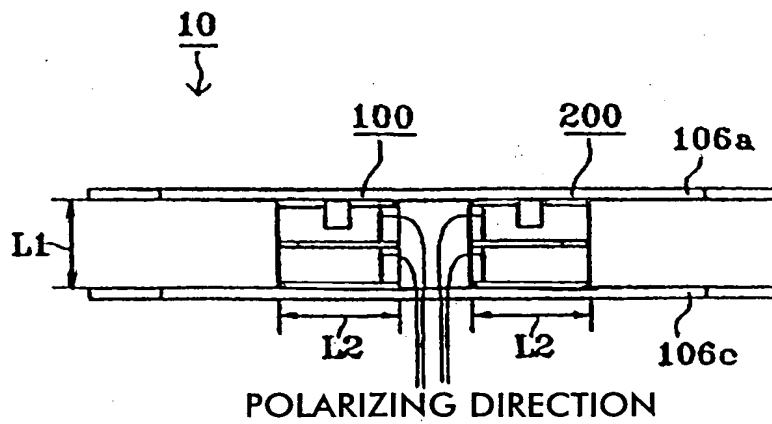


FIG. 2

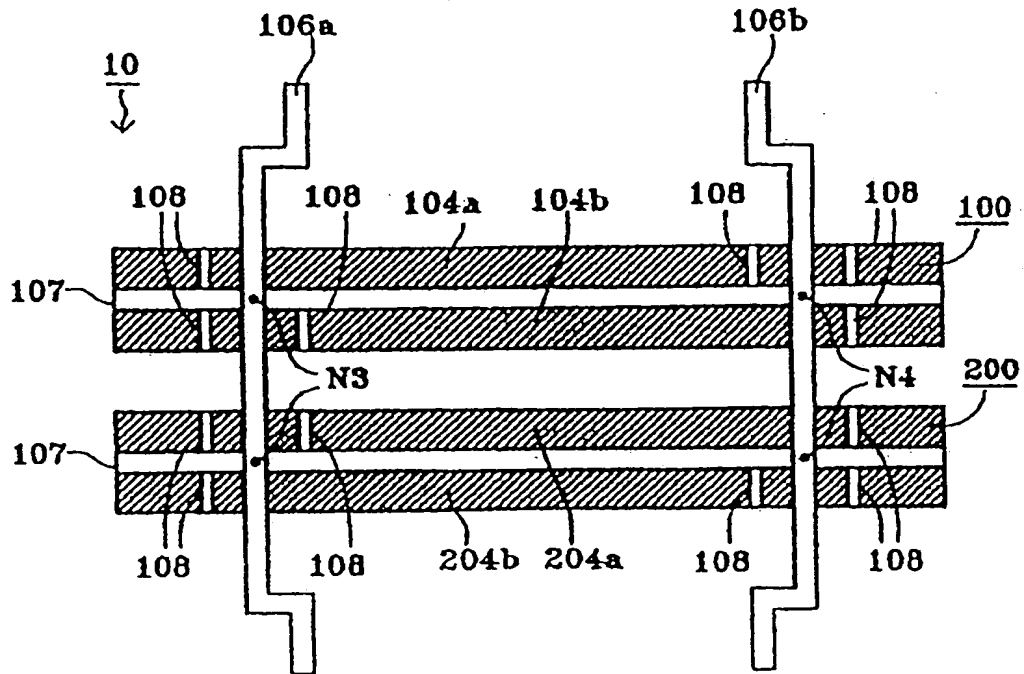


FIG. 3

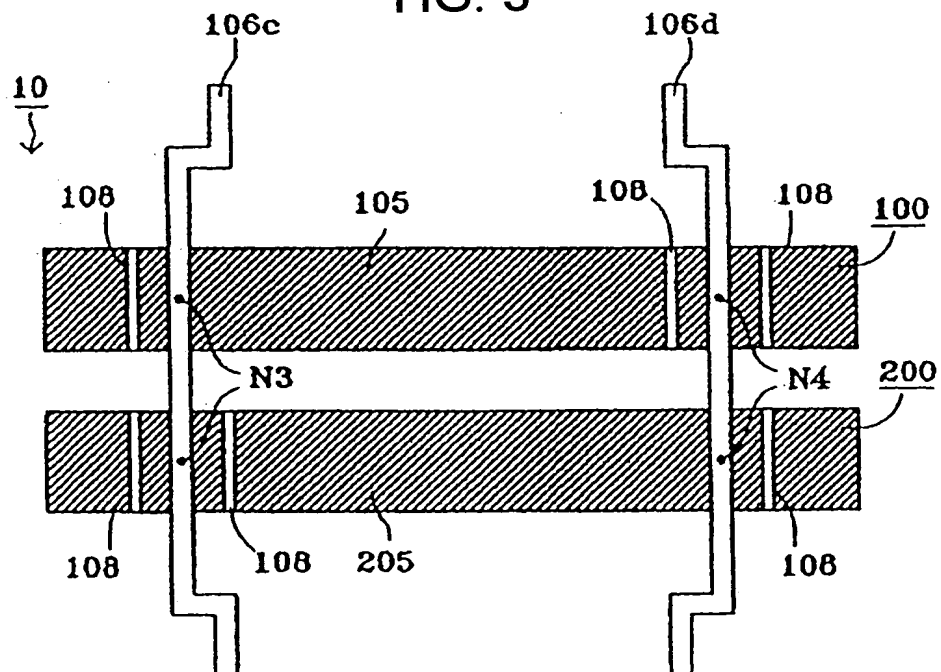


FIG. 5A

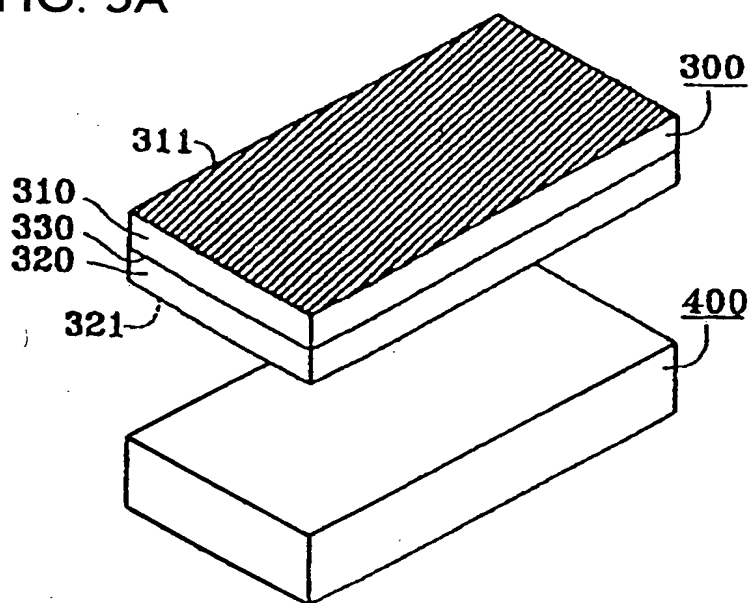


FIG. 5B

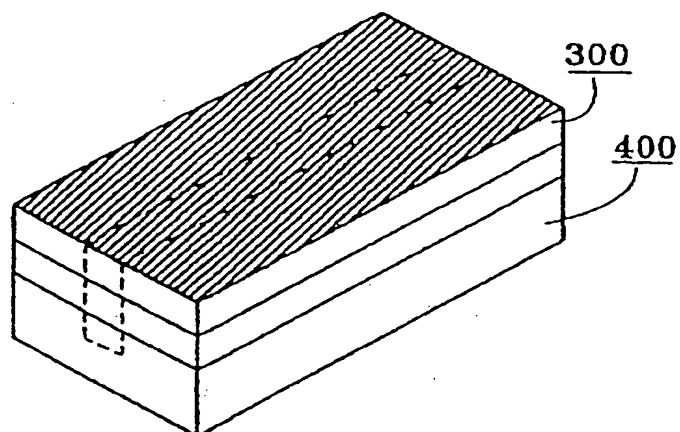
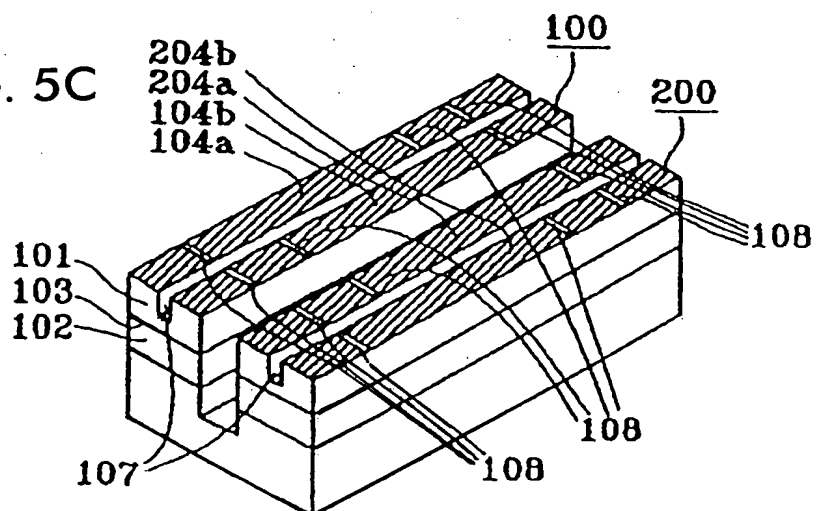


FIG. 5C



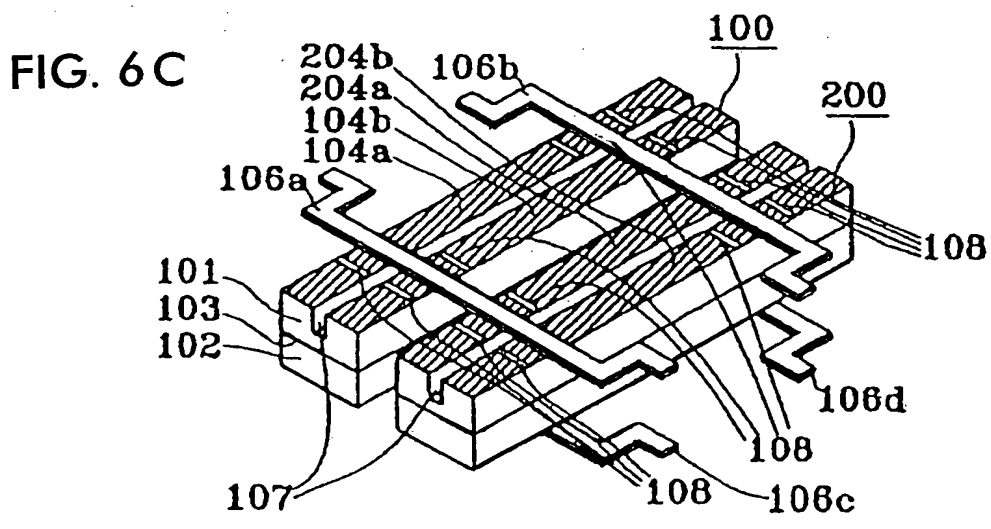
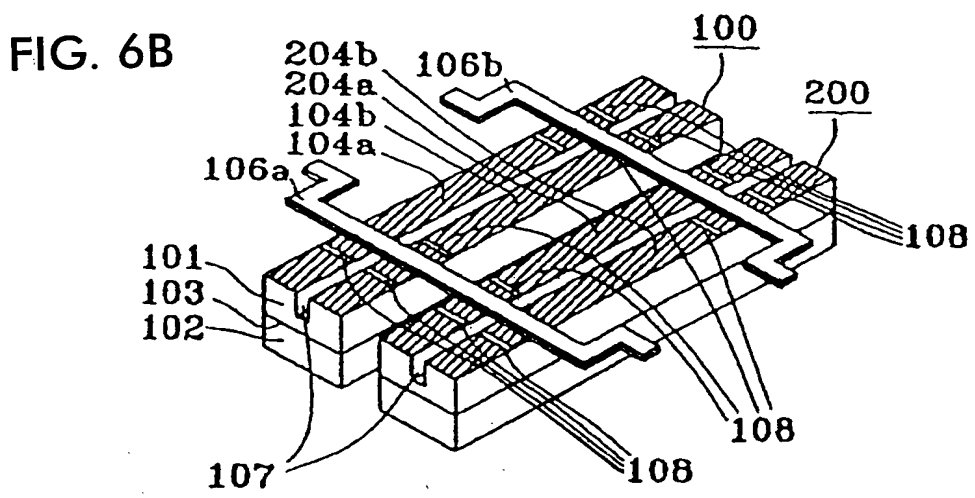
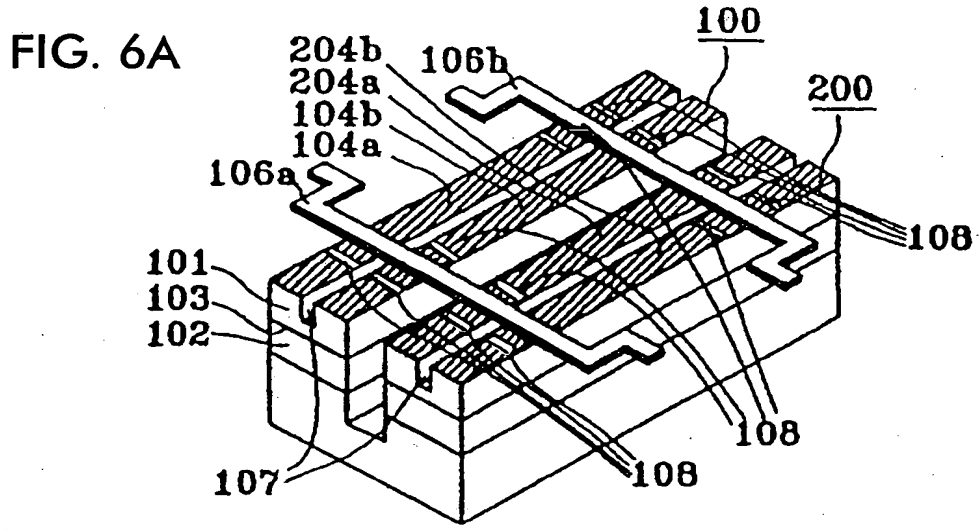


FIG. 7

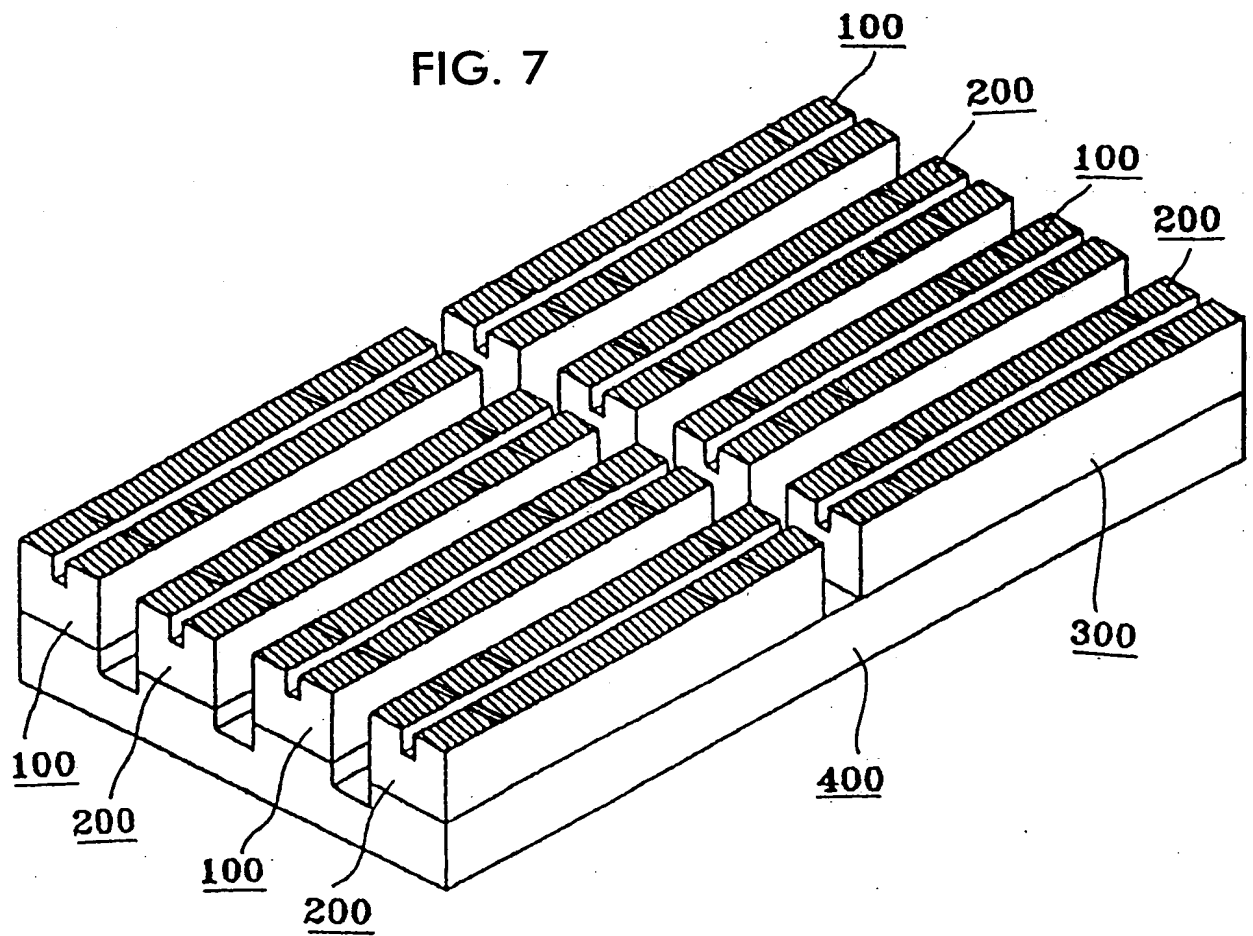


FIG. 8  
A MODE

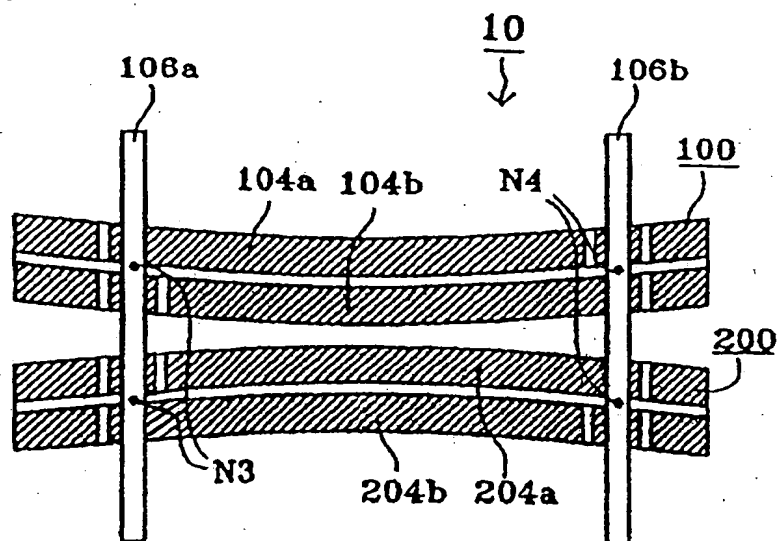


FIG. 9  
B MODE

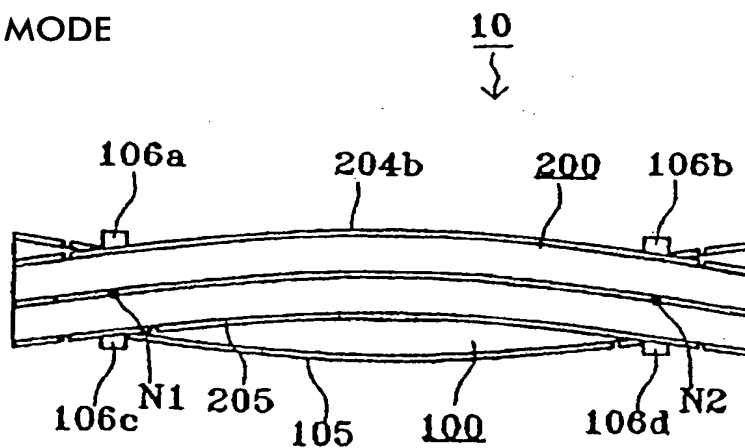


FIG. 10A

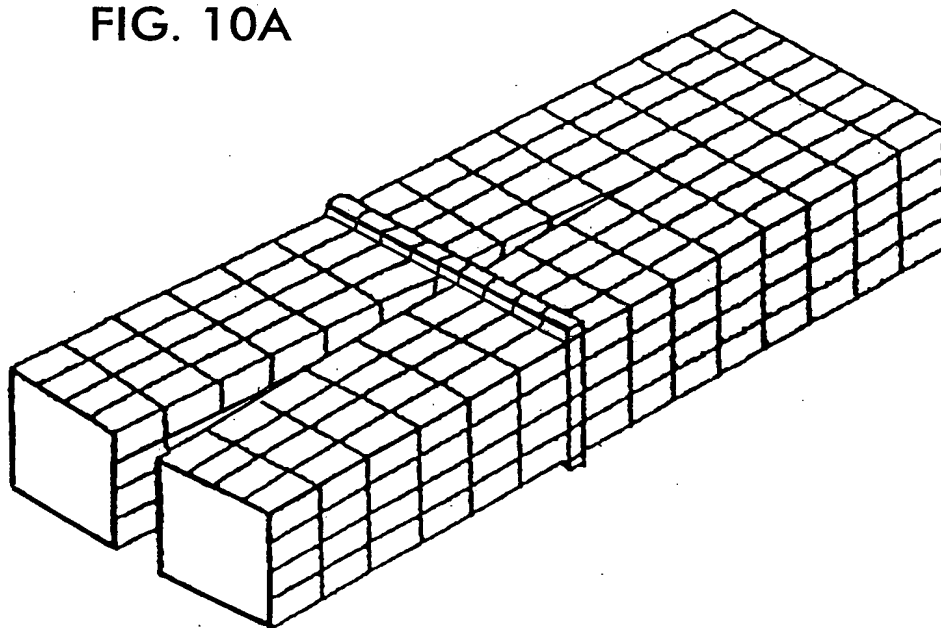
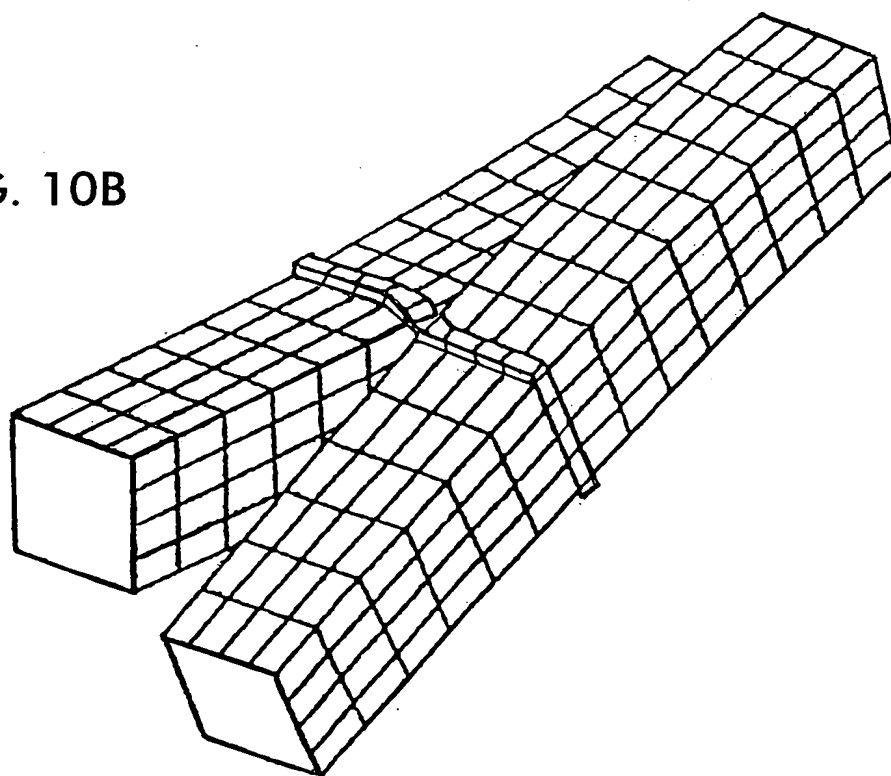


FIG. 10B



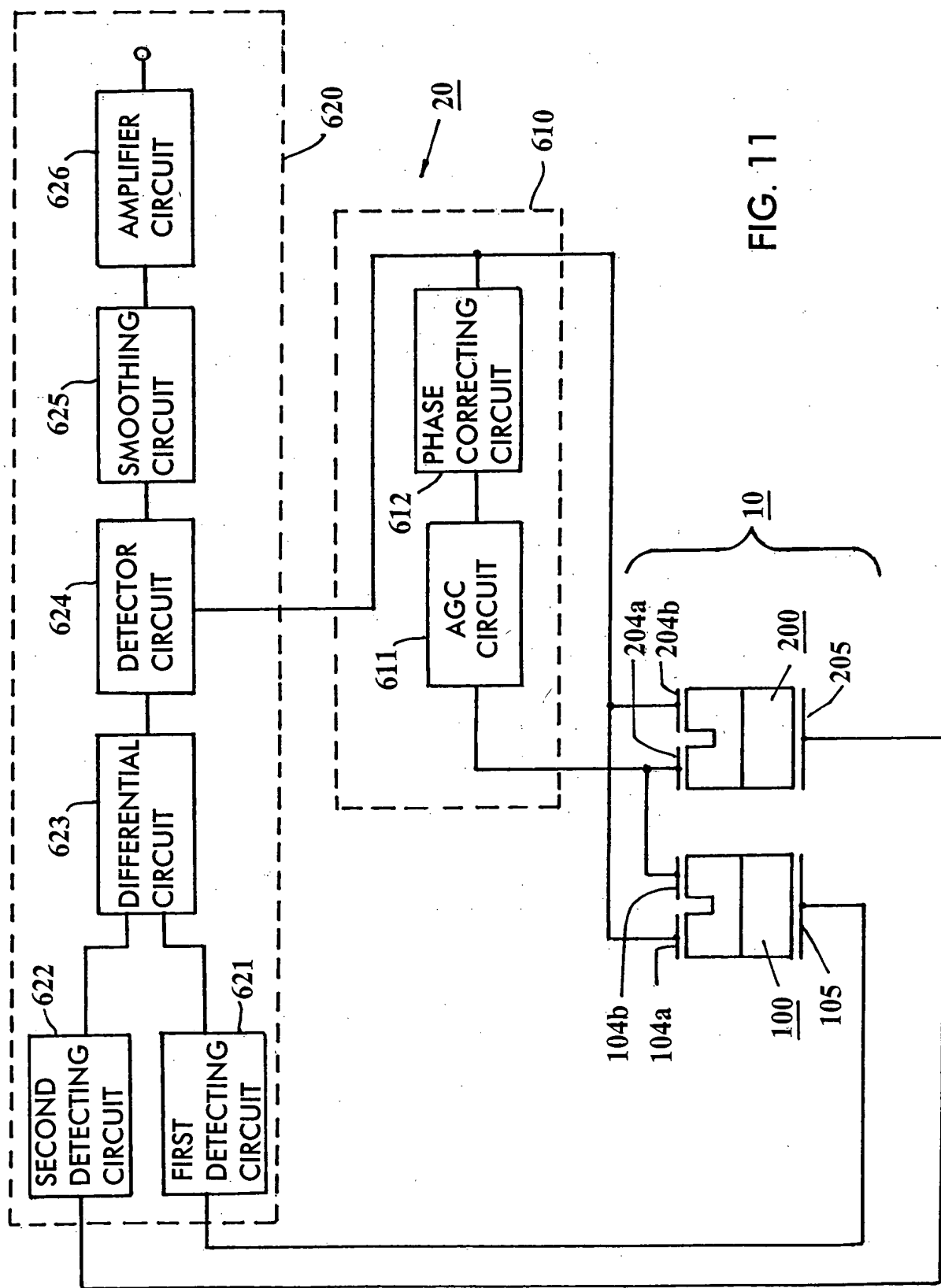


FIG. 11



This cross-sectional view shows a semiconductor device with two active regions, 100 and 200, separated by a central region. The device is built on a substrate 102. Each active region contains a stack of layers: a bottom layer 104a, a middle layer 104b, and a top layer 108. A gate stack 106 is positioned over the active regions, with gates 106a and 106b over the top layer 108, and gates 106c and 106f over the middle layer 104b. The central region is defined by gates 106a and 106b, and contains a layer 104a. The device is surrounded by a passivation layer 107. A dashed arrow 10a points to the top of the device.

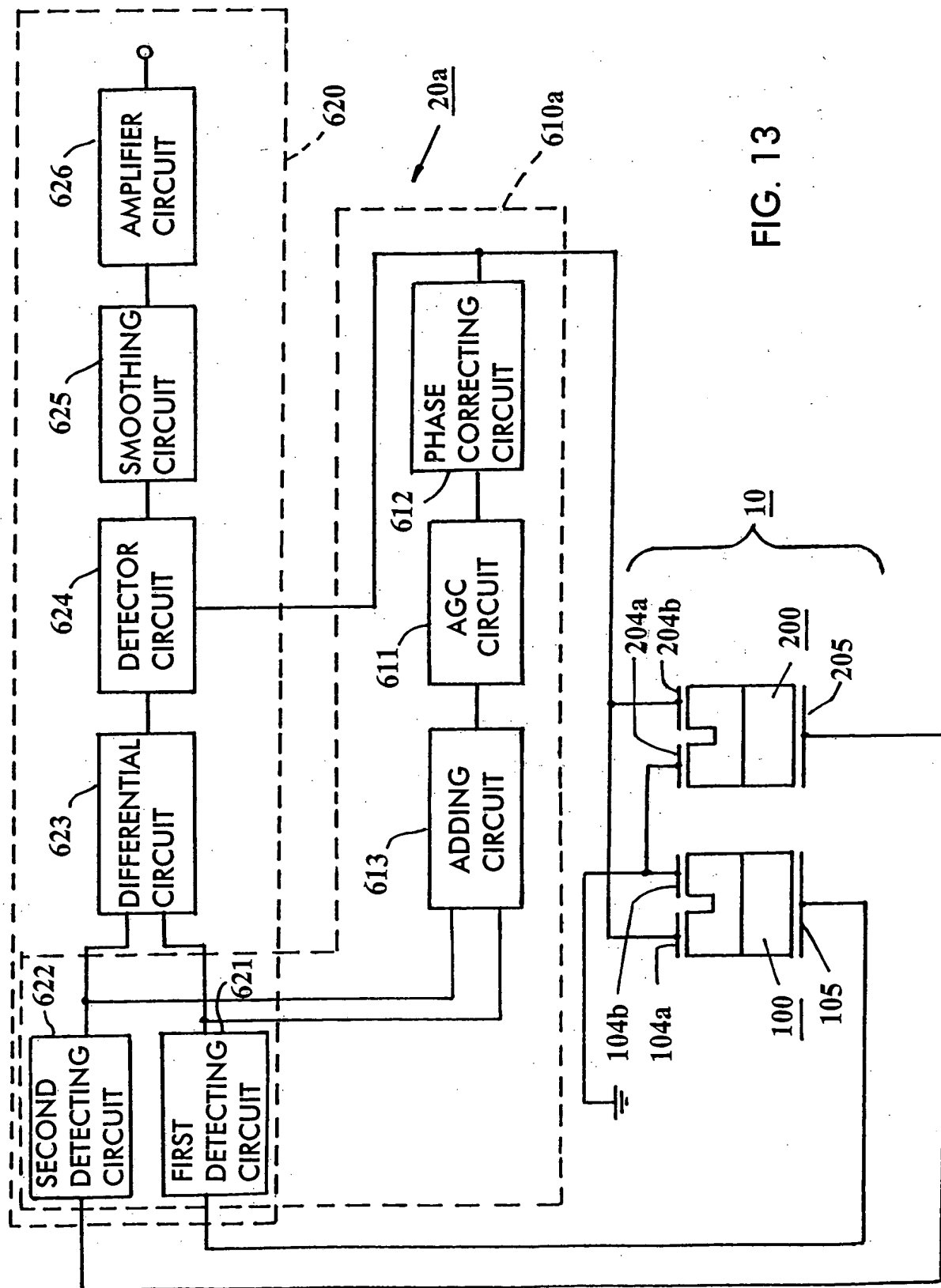


FIG. 13

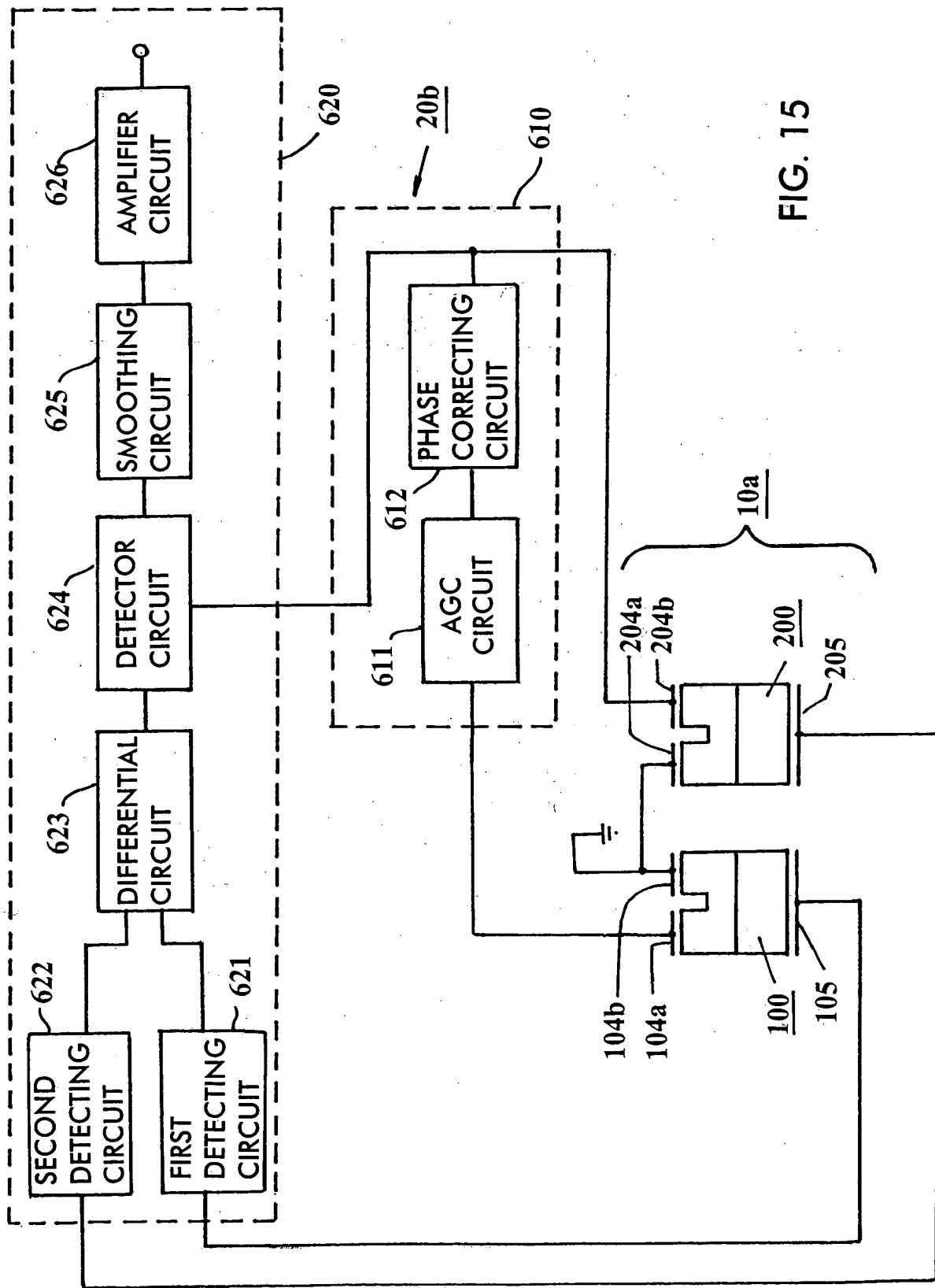


FIG. 15

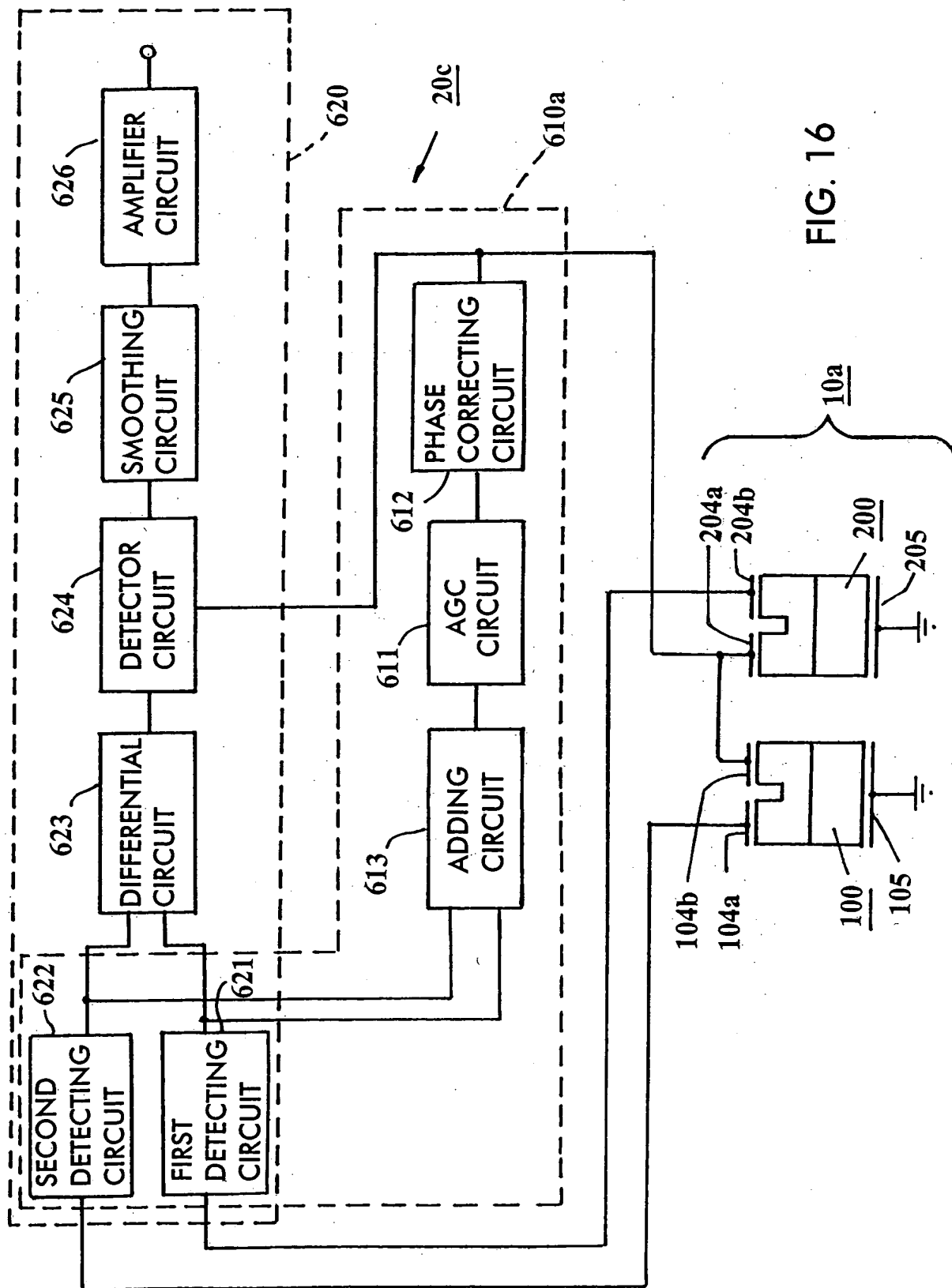


FIG. 16

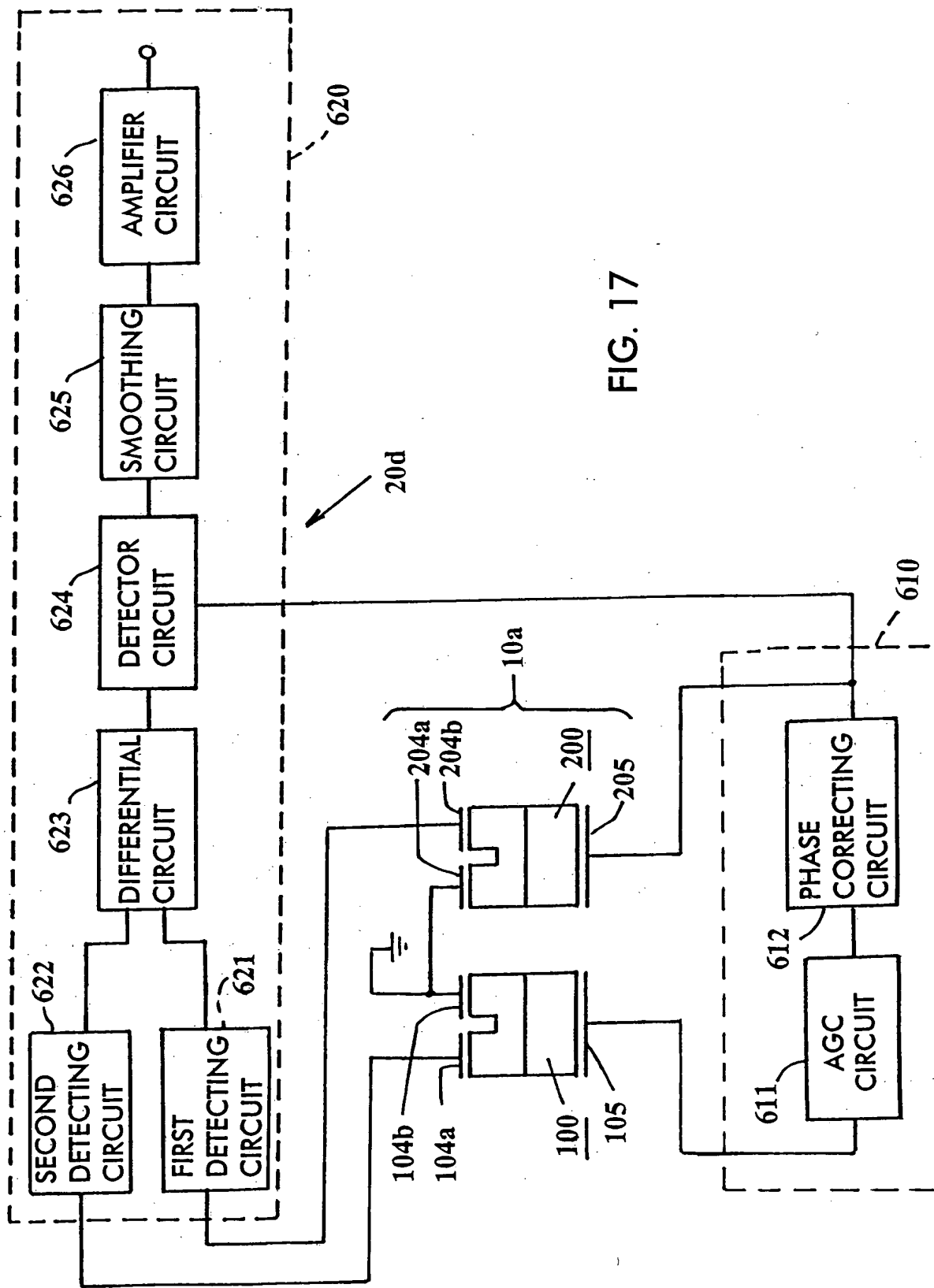


FIG. 17

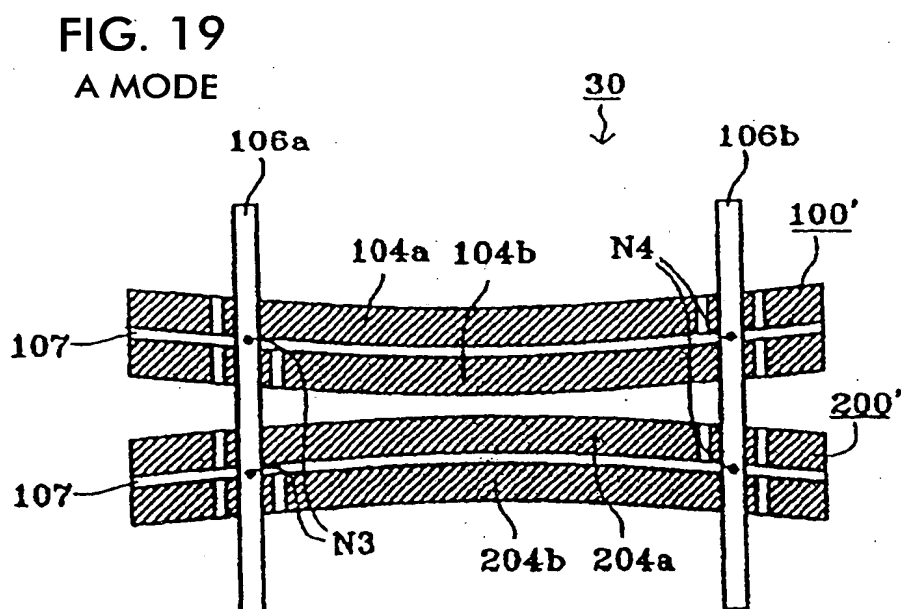
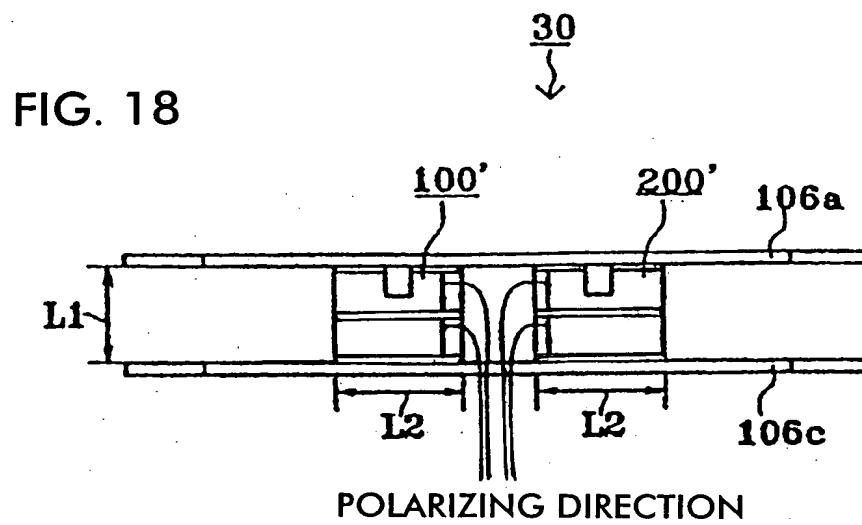
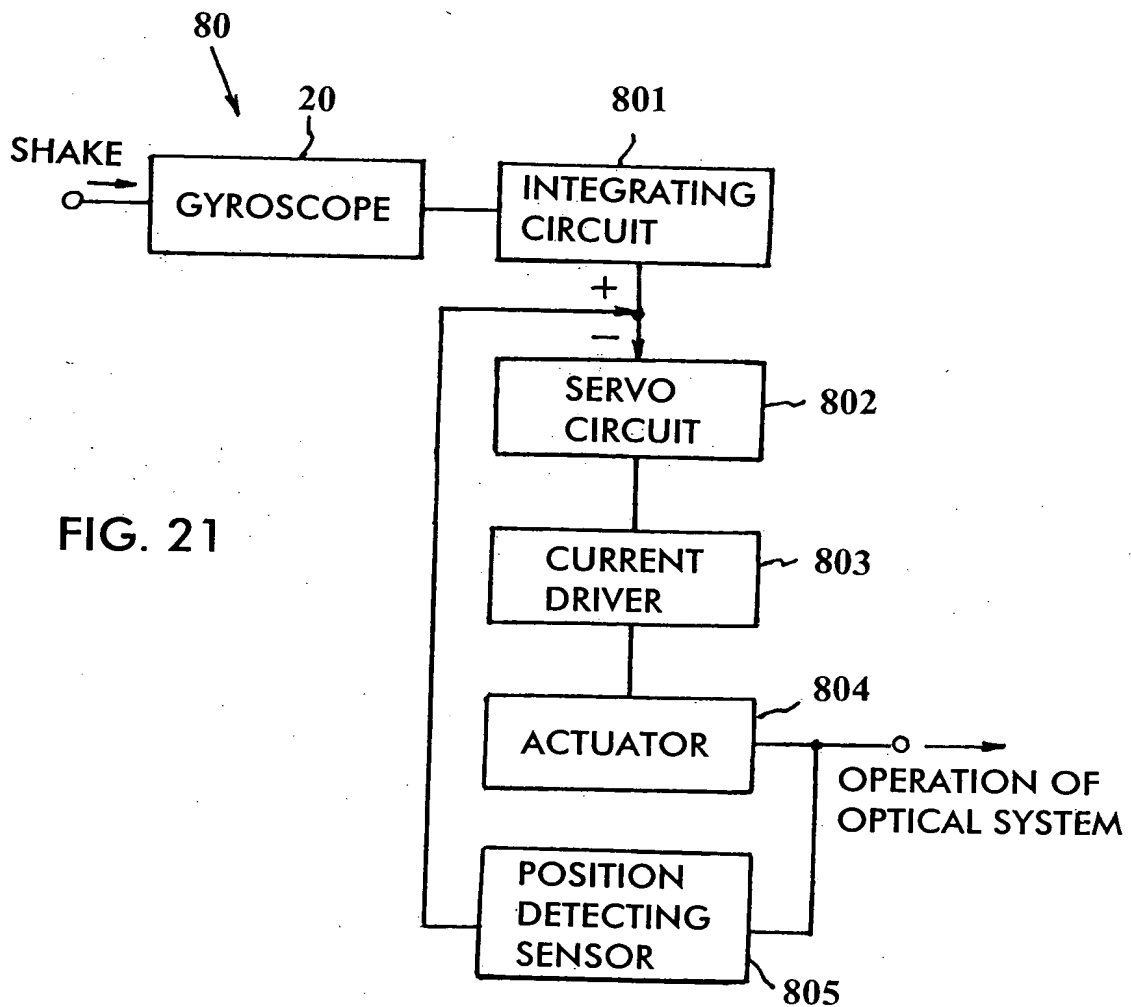
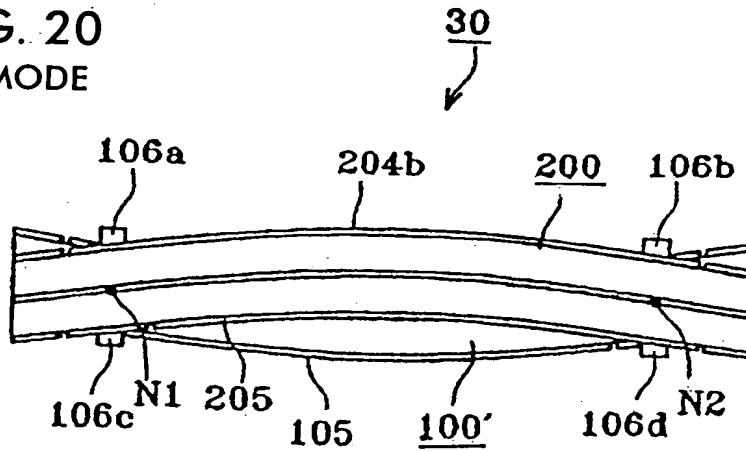


FIG. 20  
B MODE



**FIG. 22**  
PRIOR ART

